Intercept Point Behavior of Ka-Band GaAs High Power Amplifiers

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Abstract—**Intermodulation distortion (IMD) and output intercept point (OIP) behavior due to output power saturation, thermal effects and bias conditions were investigated for AlGaAs/InGaAs/GaAs pHEMT power amplifiers at Ka-Band frequencies. A power amplifier with a chip size of 3.3 mm^2 and a saturated output power of more than 27 dBm from 37 - 41 GHz, and a 3 mm^2 high gain compact dual-gate power amplifier with an output power saturation of 27 dBm at 35 GHz were designed. Intermodulation distortion for these two power amplifiers was compared. In order to separate fundamental effects from measurement induced phenomena, the principle accuracy of multi-tone measurement systems that are based on scalar spectrum analyzers was reviewed.**

I. Introduction

CURRENT millimeter-wave front ends for local multi-point distribution service (LMDS) systems still lack components with improved linearity and power added efficiency while having high output power capabilities. All of these characteristics are opposing goals to be met. In addition, addressing mass consumer markets requires inexpensive components that use smart packaging solutions and minimum GaAs chip sizes. For power amplifiers third and higher order intermodulation performance is the usual criterion for designing biasing schemes and analog linearizers in Ka-band. Two-tone intermodulation distortion also serves as an indicator for subsequent performance in real communication systems operated with digitally modulated signals.

Relationships between output intercept point (OIP), intermodulation ratio (IMR), and system level figures of merit like adjacent channel power ratio (ACPR) and noise power ratio (NPR), have been derived by using Volterra series expansions up to third order [1]. A general explanation of so called sweet spots in intermodulation distortion (IMD) of power amplifiers was given in [2], [3] and verified with a single-stage MESFET power amplifier at mobile communication bands. An improved third order output intercept point (OIP3) determined at higher output power levels for a Ka-band double recess pHEMT power amplifier for 24 - 27 GHz was observed in [4] when biased towards class A operation although in the class AB regime the P_{-1dB} compression point was better due to gain overshoot.

In this work the OIP behavior of two single recess GaAs pHEMT power amplifiers at Ka-Band frequencies is presented. Both designs were realized in coplanar technology. They employ different transistor configurations but show similar output power capabilities. We introduce the input power dependent OIPs as a visualization technique for biasing and temperature effects on IMD and show their characteristic behavior up to fifth order.

Both measurement accuracy and temperature effects are the critical impediments for established modelling approaches that are needed for optimization of the linearity of high power amplifiers on the circuit level. In [5] the effect of input amplifier distortion on IM measurements was observed. Therefore we initially give a short review of measurement accuracy of IMD with a scalar setup.

II. Measurement Accuracy

It is well known that the two main errors when determining IMR and OIP3 are uncertainty of absolute power levels at the device under test (DUT) and spurious IMD stemming from the measurement system. The former is related to the principle of scalar measurements. When good matching to 50 Ω of all components in the measurement system is guaranteed, OIPs of power amplifiers in the Ka-band can be measured on-wafer with common scalar setups to approximately 1 dB accuracy with respect to the used power reference standard. When referencing absolute power levels at the output of the system, OIP3 is not deteriorated by the additional tracking error, in contrast to measuring third order input intercept point (IIP3) for receiving components. IMD uncertainty is determined by relative spectrum analyzer accuracy and RF calibration to power meter reading under single tone excitation. In order to avoid measuring IMD with spectrally impure signal sources and overdriven receiving analyzers we chose signal sources composed of waveguide combining and isolating components in the Ka-band. Care was taken to keep power levels at the internal mixer of the spectrum analyzer below -25 dBm. The resulting OIP3 of the overall measurement system for high power amplifier testing was verified and is greater than 57 dBm for 26.5 - 40 GHz and for 33 - 50 GHz.

III. Technology and Amplifier Design

The investigated power amplifiers were fabricated using our IAF in-house double δ-doped AlGaAs/InGaAs/GaAs 0.15 μm pseudomorphic HEMT process on 4" wafers. Key features are an extrinsic maximum transconductance of 800 mS/mm at V_g = 0 V, a maximum current I_{sat} of 1000 mA/mm, off-state breakdown voltage of more than 5.5 V and a maximum extrinsic transit frequency f_T of 95 GHz at V_d = 1.5 V.

In Fig. 1 a chip photo of the compact 37 - 41 GHz power amplifier is shown. The chip size is 3.3 mm^2 including blocking capacitors of 15 pF in the bias networks. Stability analysis was performed employing symmetry devices [6]. Odd-mode suppression resistors were used to guarantee push-pull oscillation free operation. The corresponding measured and simulated output power performance at a mid band frequency of 39 GHz is presented in Fig. 2. The matching at the output was performed for optimum output power near saturation with our in-house table-based large signal model. The output stage has a total gate width of 4x8x60 μm. For a maximum output power of more than 27 dBm, an output power per chip-size of better than 150 mW/mm^2 was achieved.

Fig. 3 depicts the dual-gate power amplifier for 35 GHz radar

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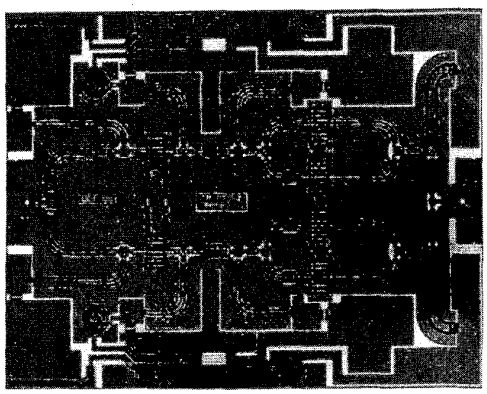

Fig. 1. Chip photo of the 40 GHz 2-stage power amplifier for LMDS applications. Chip size is 3.3 mm^2

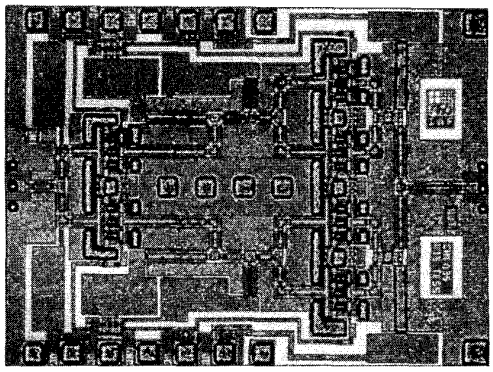

Fig. 3. Chip photo of the 35 GHz dual-gate high gain power amplifier prepared for flip-chip packaging. Chip size is 1.5 x 2 mm^2.

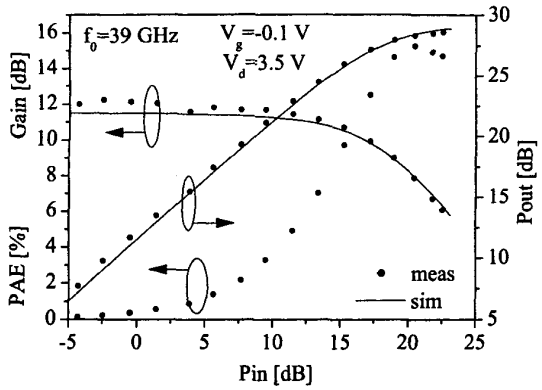

Fig. 2. Measured and simulated output power characteristic of the power amplifier at mid-band frequency (39 GHz) under one-tone excitation. Measurements were performed with a vector-corrected one-tone measurement system.

applications. The linear gain due to the use of dual-gate transistors was increased by more than 5 dB to approximately 17 dB while maintaining a saturated output power of 27 dBm. The chip size is only 3 mm^2 which resulted in an output power per chip area of better than 170 mW/mm^2 in saturation. Both amplifiers are designed for building high power amplifier modules composed of several small amplifier cells mounted on AlN with the IAF in-house flip-chip technology. In Fig. 3, the galvanic grown bumps around the dual-gate transistors and on their source islands can be seen.

IV. Measurement Results and Discussion

In this section the two-tone intermodulation measurement results of the dual-gate and common source power amplifiers are compared.

As a first rule of thumb, amplifier distortion in the quasi-small-signal regime is often predicted by employing third order power series to approximate the behavior of the nonlinear voltage controlled output current generator. In doing so, a unilateral input-output relationship is assumed. Sometimes the IMD generation mechanisms on the input side of field-effect transistors are considered by applying the same method to the nonlinear gate-source capacitance. We refer to this as the classical theory. When using this classical theory for two-tone excitation of equal power, one can derive a fixed figure of merit, the output intercept point, that allows one to calculate the intermodulation distortion levels of third and higher order for arbitrary output power levels by the simple relationship

$$\mathrm{OIP}n = \frac{n}{n-1}P_{f_0} - \frac{1}{n-1}\mathrm{IMD}n \qquad (1)$$

In Eq. (1) n expresses the order of the intercept point which is the sum of the integers $k+l$ when calculating the spectral intermodulation component $kf_0 \pm lf_1$. This concept is well known and a popular means to quantify the non-linearities disturbing neighboring channels in communication systems.

However, one can see in various amplifiers that intermodulation distortion does not follow the classical theory even not near the small-signal regime. In addition, cancellation effects in IMD3 and IMD5 behavior might be observed when going to larger input power levels. These so called sweet spots can be described by an expansion of the power series approach up to the 5th or 7th order [7] and lead to a more complete theory with respect to the above described model. In this case, the OIP is not independent of the input power level anymore and its meaning in the sense of the classical theory is lost. There are two ways to apply the OIP concept nevertheless. One can determine the intersection between the third order intermodulation distortion and the output power of one fundamental by extrapolation from the small-signal regime. However, this leads to icorrect results when deriving IMRs from the OIP by assuming Eq. (1). The other way is to apply directly Eq. (1) to calculate the OIP at one input power level. For the non-classical case, it follows that the OIP is only useful when we know the input or output power level that it was calculated for. When the OIP obtained in this manner is plotted as a function of the input power, it can be seen where the OIP concept holds. In communication applications one is mainly interested in the maximum output power that can be achieved while maintaining a certain distance to spurious adjacent tones. Therefore it is more concrete to show IMR as a function of the output power.

We will start with the discussion of the power amplifier cell

composed of common source transistors.

Fig. 4 depicts the dependency of the lower OIP3 and OIP5 behavior on the input power level for different gate voltages and a fixed drain voltage at V_d = 3.5 V. Indicated in the diagram by

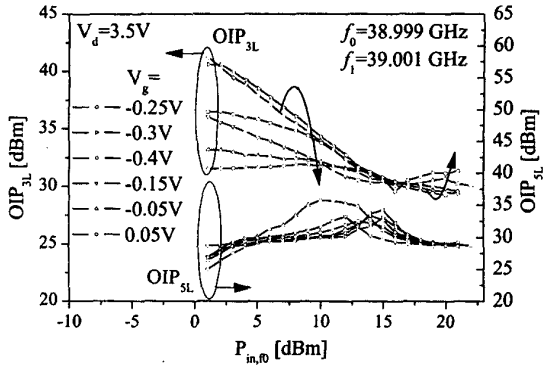

Fig. 4. Input power dependent *lower* 3rd and 5th order OIP for the common source cell at V_d = 3.5 V. Parameter is the gate-source voltage V_g.

an arrow, the OIP3 is showing a maximum in the small-signal regime at approximately V_g = -0.3 V when going from class A operation points to the class AB regime. At the same time, cancellation effects in the IMD5 are growing and shifting towards higher input power levels. This results in a peaking of OIP5. When increasing input power levels to the saturation regimes, the bias dependency is fading because of the dominance of clipping effects and self-biasing. In class AB operation the OIP concept for classical theory does not even hold for the quasi-linear operation region. However, the OIP3 calculated this way reaches values that are better by 10 dB at around V_g = -0.3 V when compared to the operation in class A mode. For high input power levels, the class A operation shows better performance than the class AB operation, although the P_{-1dB} point under single-tone excitation is worse (not shown in diagrams).

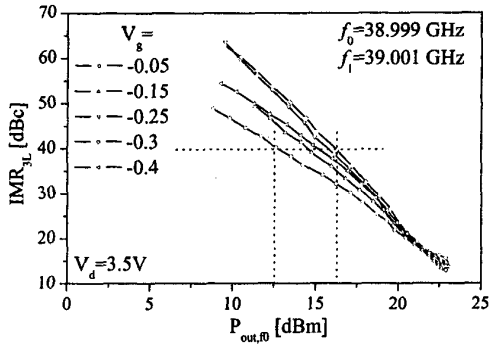

Fig. 5. *Lower* 3rd order IMR as a function of the output power of one fundamental tone at V_d = 3.5 V. Parameter is the gate-source voltage V_g.

In Fig. 5, the IMR3 as function of the output power is plotted for the same bias conditions up to P_{-1dB} at about 20 dBm per tone under two-tone excitation. Now an improvement in output power for a specified IMR3 can be achieved when biasing this power amplifier in a class AB operation mode. For example a 3.7 dB higher output power is achieved at IMR3 = 40 dBc. At near saturation the class A regime leads to a better IMR3 performance but the IMR3 levels are too low for communication system applications.

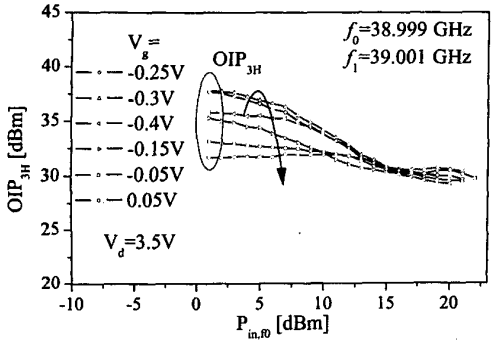

Fig. 6. Input power dependent *upper* 3rd order OIP for the common source cell at V_d = 3.5 V. Parameter is the gate-source voltage V_g.

In Fig. 6 the upper OIP3 is shown. Compared to Fig. 4, the lower and upper OIP3 is not the same due to memory effects. It can be observed that these effects are getting more pronounced and reach a maximum for optimum small-signal OIP3 bias conditions when going from class A towards class AB operation. Finally we demonstrate the temperature effects on the OIPs by Fig. 7. It is quite obvious that OIPs are decreasing with increasing temperature. Particularly when looking at the OIP5, the decrease of the nulling effect is noticed.

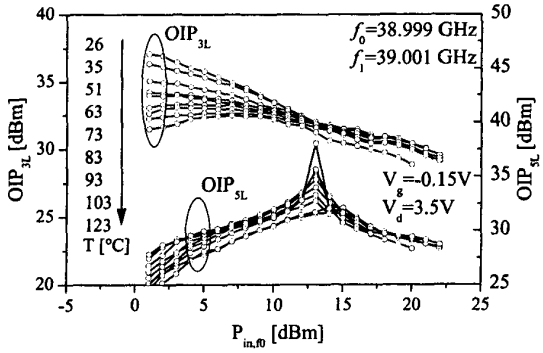

Fig. 7. Input power dependent *lower* 3rd and 5th order OIP for the common source cell at V_d = 3.5 V. Parameter is the temperature.

Now we look at the dual-gate power amplifier. It is of particular interest since the additional voltage control at the transistor (second gate voltage) gives another degree of freedom but makes it more difficult to find an optimum bias condition for intermodulation behavior and output power performance. Again the input power level dependent OIP is used to investigate the limits of the OIP concept.

In Fig. 8, the drain bias dependency for typical bias conditions of the two gate voltages is illustrated. The OIP3 is increasing with the drain voltage in the quasi-small-signal regime by approximately 4 dB when changing drain voltage from 4.0 V to 5.0 V. As for the common source power cell, only slight changes can be seen when the first gate is biased near class A operation and the drain voltage is increased. However, at V_g = -0.15 V near class AB operation the effects get more obvious. Uniquely

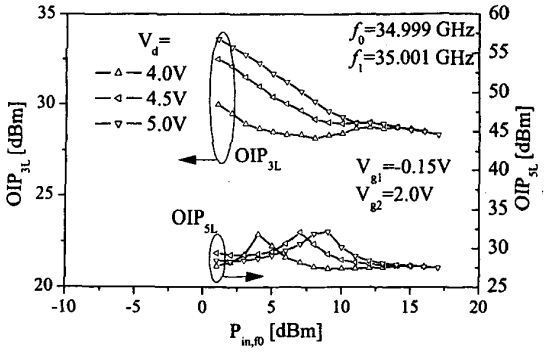

Fig. 8. Input power dependent *lower* 3rd and 5th order OIP for the dual-gate power cell. The two gate voltages are fixed to a typical bias point of V_{g1} = -0.15 V and V_{g2} = 2.0 V. Parameter is the drain bias voltage V_d.

for the dual-gate configuration is the bias constellation that can be observed when the drain voltage is kept quite low and the first gate is chosen at an intermediate point between class A and class AB operation. This is depicted in Fig. 9. When the second

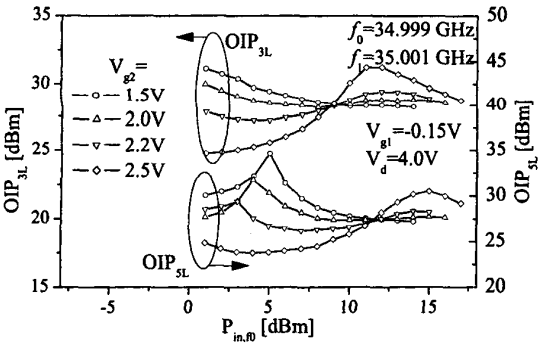

Fig. 9. Input power dependent *lower* 3rd and 5th order OIP for the dual-gate power cell. V_d = 4.0 V. Parameter is the second gate bias voltage V_{g2}.

gate voltage is increased, the OIP3 behavior is improved for the large signal regime and it is worsened for the quasi-small-signal region. All the curves are intersecting at one point for OIP3 and OIP5. Although there is a memory effect, the intersecting points remain the same for lower and upper OIPs (not shown in diagrams). This behavior allows to tune for better linearity performance at higher input power levels at the cost of decreased IMD performance at lower input power levels.

The respective IMR3 behavior is shown in Fig. 10. The output power level at a specified IMR3 drops below the corresponding value for the common source amplifier. However, it can be improved by several dB when choosing an optimal bias point.

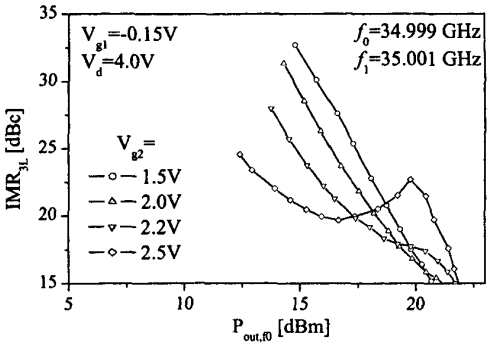

Fig. 10. 3rd order IMR as a function of the output power of one fundamental tone. First gate bias voltage is V_g = -1.5 V. Drain bias voltage is V_d = 4.0 V. Parameter is the second gate (cascode) bias voltage V_{g2}.

V. Conclusions

OIP3 and OIP5 behavior in single recess GaAs pHEMT power amplifiers were investigated. The concept of output intercept point was extended to visualize the strong input power level dependency of this figure of merit. Biasing in a class AB scheme allows to improve output power capabilities in common source configuration with respect to class A operation by 3.7 dB at 40 dBc IMR3 for the common source power amplifier and at least 4 dB for the dual-gate power amplifier respectively.

VI. Acknowledgments

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